Analysis of Intrinsic Noise for 3T CMOS Voltage References

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***Abstract*— In view of the ultra-low-power (ULP) consumption that is often demanded in internet-of-things (IoT) applications, several CMOS voltage reference circuits have been reported consuming from picowatt down to femtowatt powers. Such ULP performance is achieved by biasing transistors using extremely low currents. In this way, the lower is the bias current the higher the intrinsic thermal noise is, and its influence on the design cannot be neglected. In this paper, analytical expressions for both thermal and flicker noises for 3-transistor (3T) voltage references are advanced in order to quantify the intrinsic noise influence on the circuit performance. The results were validated by extensive simulations with HSPICE using a 180 nm CMOS process.**

Keywords*— *Intrinsic noise, low voltage, sub-threshold, ultra low power, voltage reference.

I. Introduction

A voltage reference circuit is used in most analog, digital, and mixed-signal systems-on-chips (SoCs). Its insensitivity to temperature and supply voltage variations makes this circuit a crucial block for many applications, such as, digital-to-analog and analog-to-digital converters, sensors, among other devices. Due to the continuous growing of internet-of-things applications, several voltage reference circuits that consume from picowatt down to femtowatt have been widely reported in recent years [1]–[3].

In this paper analytical expressions of the intrinsic noise for 3T voltage reference circuits are advanced in order to evaluate their influences on the output voltage. The paper is organized as follows: Section II derives the thermal and flicker noise analyses, and applies the resulting models to determine the total noise of the reference voltage. Section III presents simulation results compared with the predicted ones obtained by using analytical expressions. Concluding remarks are made in Section IV.

II. Intrinsic noise of 3T Voltage Reference

A. Small-Signal Modeling of 3T Voltage Reference

In order to analyze the intrinsic noise produced by transistors in the 3T voltage reference circuit (see Fig. 1), a small-signal representation of the circuit is required. Fig. 2 presents the small-signal model of the voltage reference. It should be noted that since the gate of transistor M_3 is connected to its source terminal, the small-signal that is dependent on the current source was neglected.

B. Thermal Noise

According to [4], [5], the power-spectral density (PSD) of the current noise, for saturated transistors in weak inversion, is given by

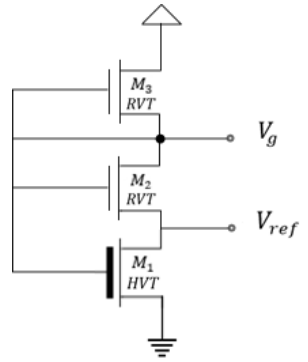

Fig. 1. Schematic circuit of 3T voltage reference [1,2].

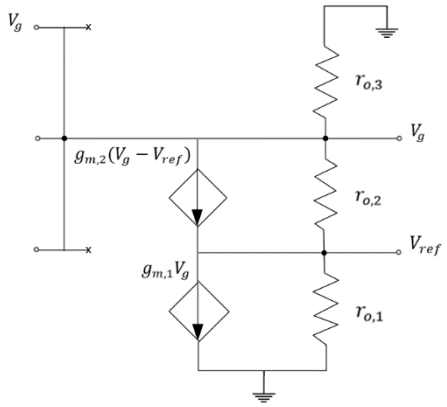

Fig. 2. Small-signal model of the 3T voltage reference.

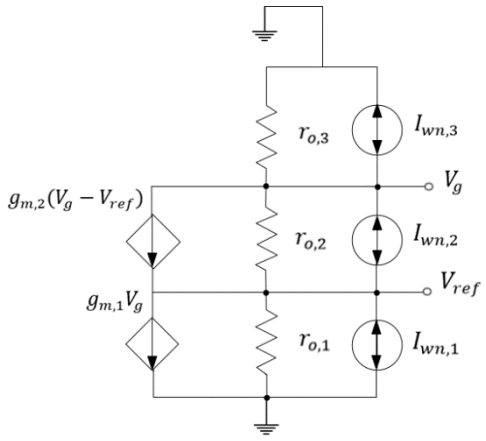

Fig. 3. Small-signal model including thermal noise current sources.

$$S_{wn,i} = I_{wn,i}^2 = 2K_B T n g_{m,i} \quad (1)$$

where K_B is the Boltzmann constant, T is the absolute temperature, n is the slope factor, and $I_{wn,i}$ and $g_{m,i}$ are, respectively, the equivalent noise current source and the transistor transconductance M_i (i = 1, 2, 3).

Fig. 3 shows the small-signal model of the 3T voltage reference by including the equivalent thermal noise current sources. In order to determine the total output thermal noise, the contribution of each current source to the output can be analyzed separately by using the superposition theorem.

By applying nodal analysis for the circuit of Fig. 3, it is possible to find the gain $V_{ref}/I_{wn,i}$ (i = 1, 2, 3) for each noise current source. It is important to note in Fig. 3 that $r_{o,i} = 1/g_{ds,i}$, where $g_{ds,i}$ is the drain to source conductance of transistor M_i.

1) Analysis for the determination of $V_{ref}/I_{wn,3}$

By only considering the thermal noise contribution of M_3, the circuit is determined by the following equation system

$$\frac{-V_g}{r_{o,3}} + I_{wn,3} = \frac{V_g - V_{ref}}{r_{o,2}} + g_{m,2}(V_g - V_{ref}) \quad (2)$$

$$\frac{V_{ref}}{r_{o,1}} + g_{m,1}V_g = \frac{V_g - V_{ref}}{r_{o,2}} + g_{m,2}(V_g - V_{ref}). \quad (3)$$

Then, by substituting Eq. (2) into Eq. (3), we obtain Eq. (4).

2) Analysis for the determination of $V_{ref}/I_{wn,2}$

On the other hand, by considering only the thermal noise contribution from M_2, we obtain

$$\frac{-V_g}{r_{o,3}} = \frac{V_g - V_{ref}}{r_{o,2}} + g_{m,2}(V_g - V_{ref}) + I_{wn,2} \quad (5)$$

$$\frac{V_{ref}}{r_{o,1}} + g_{m,1}V_g = \frac{V_g - V_{ref}}{r_{o,2}} + g_{m,2}(V_g - V_{ref}) + I_{wn,2} \quad (6)$$

from which substituting Eq. (5) into Eq. (6), we obtain Eq. (7).

3) Analysis for the determination of $V_{ref}/I_{wn,1}$

Finally, by considering only the thermal noise contribution from M_1, the resulting equation system yields

$$\frac{-V_g}{r_{o,3}} = \frac{V_g - V_{ref}}{r_{o,2}} + g_{m,2}(V_g - V_{ref}) \quad (8)$$

$$\frac{V_{ref}}{r_{o,1}} + g_{m,1}V_g + I_{wn,1} = \frac{V_g - V_{ref}}{r_{o,2}} + g_{m,2}(V_g - V_{ref}). \quad (9)$$

Substituting Eq. (8) into Eq. (9), we obtain Eq. (10).

Once the analysis is made on subthreshold operation, the transconductance over the drain current ratio can be approximated by $1/(nU_T)$ [6]. In fact, since the currents through M_1, M_2 and M_3 are equal, we can assume that the transconductances are also equal, that is, $g_{m,1} = g_{m,2} = g_{m,3} = g_m$. Therefore, the total PSD of the noise voltage can be estimated by applying the superposition theorem, that is,

$$S_{wn} = S_{wn,1}\left(\frac{V_{ref}}{I_{wn,1}}\right)^2 + S_{wn,2}\left(\frac{V_{ref}}{I_{wn,2}}\right)^2 + S_{wn,3}\left(\frac{V_{ref}}{I_{wn,3}}\right)^2. \quad (11)$$

Eq. (12) provides a complete version of Eq. (11), which includes the circuit parameters. Therefore, the total RMS thermal noise of the reference voltage is given by

$$V_{wT} = \int_{0^+}^{f_P} S_{wn}\, df, \quad (13)$$

where f_P is the dominant pole frequency.

C. Flicker Noise

Similar procedure as that of the thermal noise analysis, in order to calculate flicker noise all, the contributions from flicker noise sources should be analyzed for all transistors of the voltage reference, since such noise is present only for low frequencies.

$$S_{Fn,i} = I_{Fn,i}^2 = g_{m,i}^2 \frac{K_{F,i}}{W_i L_i} \frac{1}{f} \quad (14)$$

where, K_F is the flicker noise constant, W_i and L_i are, respectively, the width and length of transistor M_i, f is the frequency and $g_{m,i}$ are transcondutances of transistors M_i, i = 1, 2, 3.

Since the flicker noises were analyzed as current sources, similarly as made for thermal noises, the corresponding gains for the flicker sources are equal to those of the thermal gains, that is, $V_{ref}/I_{Fn,i} = V_{ref}/I_{wn,i}$, ($i$ = 1, 2, 3). For this analysis, the PSD of flicker noise is

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$$\frac{V_{ref}}{I_{wn,3}} = \frac{(g_{ds,1} + g_{ds,2} + g_{m,2})}{g_{ds,1}(g_{ds,2} + g_{ds,3} + g_{m,2}) + g_{ds,2}g_{ds,3} + g_{ds,2}g_{m,1} + g_{ds,3}g_{m,2} + g_{m,1}g_{m,2}} \quad (4)$$

$$\frac{V_{ref}}{I_{wn,2}} = \frac{(g_{ds,3} + g_{m,1})}{g_{ds,1}(g_{ds,2} + g_{ds,3} + g_{m,2}) + g_{ds,2}g_{ds,3} + g_{ds,2}g_{m,1} + g_{ds,3}g_{m,2} + g_{m,1}g_{m,2}} \quad (7)$$

$$\frac{V_{ref}}{I_{wn,1}} = \frac{-(g_{ds,2} + g_{ds,3} + g_{m,2})}{g_{ds,1}(g_{ds,2} + g_{ds,3} + g_{m,2}) + g_{ds,2}g_{ds,3} + g_{ds,2}g_{m,1} + g_{ds,3}g_{m,2} + g_{m,1}g_{m,2}} \quad (10)$$

$$S_{wn} = 2KTngm\left(\frac{(g_{ds,1} + g_{ds,2} + g_m)^2 + (g_{ds,3} + g_m)^2 + (g_{ds,2} + g_{ds,3} + g_m)^2}{(g_{ds,1}(g_{ds,2} + g_{ds,3} + g_m) + g_{ds,2}g_{ds,3} + g_{ds,2}g_m + g_{ds,3}g_m + {g_m}^2)^2}\right) \quad (12)$$

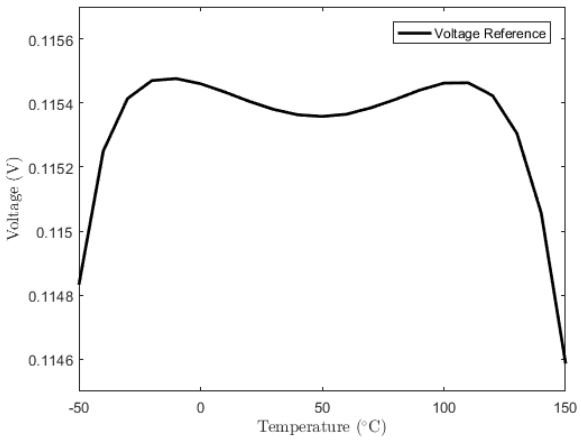

Fig. 4. Voltage reference operating from -50 ºC to 150 ºC.

$$S_{Fn} = S_{Fn,1}\left(\frac{V_{ref}}{I_{Fn,1}}\right)^2 + S_{Fn,2}\left(\frac{V_{ref}}{I_{Fn,2}}\right)^2 + S_{Fn,3}\left(\frac{V_{ref}}{I_{Fn,3}}\right)^2. \quad (15)$$

An extended expression of Eq. (15) is presented in Eq. (16). The total RMS flicker noise of the reference voltage can thus be obtained as

$$V_{FT} = \int_{0^+}^{f_P} S_{Fn}\, df. \quad (17)$$

D. Total Noise

In order to determining the total noise, it is necessary to estimate the dominant pole (f_P), which includes the total capacitance at the output node (see Table I). The analytical pole frequency is expressed in Eq. (18), which yields $f_P = 11.11$ Hz. By integrating the PSDs of the thermal Eq. (13) and flicker Eq. (17) noises, it is possible to obtain the total noises produced by the voltage reference, $V_{wT} = 99.39\ \mu V$, $V_{FT} = 5.56\ \mu V$ and $V_{nT} = \sqrt{{V_{wT}}^2 + {V_{FT}}^2} = 99.55\ \mu V$, where V_{nT} denotes the total RMS noise. It can be observed that the flicker noise has an insignificant contribution to the total noise. Table II shows the thermal noise contributions of transistors M1, M2, M3 on the reference voltage.

III. Simulation Results

The reference circuit was designed to operate in the range from −50 °C to 150 °C and minimum supply of 250 mV. The total noise was analyzed at 27 °C. Simulation results were carried by using a 180 nm CMOS process in HSPICE.

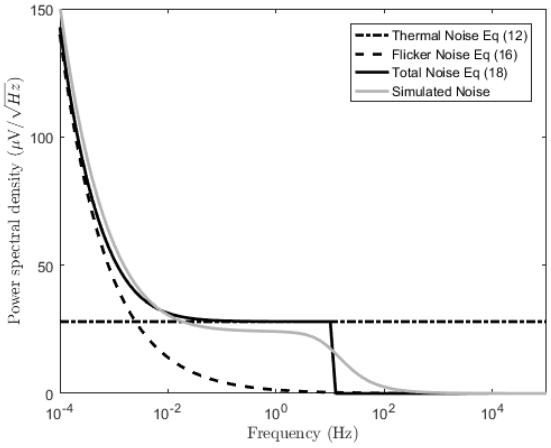

Fig. 5. Analysis of the PSD's obtained through the theoretical model and simulation in the software.

TABLE I
TABLE WITH THE DATA USED IN THE MODELING AND SIMULATION OF THE CIRCUIT

Symbol	Definition	Assumed Value
g_m	Transconductance of M1, M2 and M3	27.8 pS
$g_{ds,1}$	conductance M1	0.89 fS
$g_{ds,2}$	conductance M2	46.9 pS
$g_{ds,3}$	conductance M3	0.14 pS
n	slope factor	1.24 V/V
T	absolute temperature	300 K
K	Boltzmann constant in weak inversion	1.38e-23 J/K
$K_{F,1}$	flicker noise constant of M1	78.78e-24 m²V²/Hz
$K_{F,2}$	flicker noise constant of M2	5.11e-24 m²V²/Hz
$K_{F,3}$	flicker noise constant of M3	7.35e-24 m²V²/Hz
W_1	width M1	1.29 µm
W_2	width M2	3.45 µm
W_3	width M3	2.48 µm
L_1	length M1	32.3 µm
L_2	length M2	33.7 µm
L_3	length M3	32.9 µm
C_L	Total Output Capacitance	400 fF

S = siemens, Ω = ohm, K = kelvin, J = joule V = volt, m = meter, Hz = hertz, F = farad.

Fig. 4 shows the behavior of the voltage reference circuit along the temperature range.

$$S_{Fn} = \frac{{g_m}^2}{f}\frac{\left(\frac{K_{F,1}}{W_1 L_1}(g_{ds,2}+g_{ds,3}+g_m)^2 + \frac{K_{F,2}}{W_2 L_2}(g_{ds,3}+g_m)^2 + \frac{K_{F,3}}{W_3 L_3}(g_{ds,1}+g_{ds,2}+g_m)^2\right)}{(g_{ds,1}(g_{ds,2}+g_{ds,3}+g_m)+g_{ds,2}(g_{ds,3}+g_m)+g_{ds,3}g_m+{g_m}^2)^2} \quad (16)$$

$$f_P = \frac{g_{ds,1}g_{ds,2}+g_{ds,1}g_{ds,3}+g_{ds,1}g_m+g_{ds,2}g_{ds,3}+g_{ds,2}g_m+g_{ds,3}g_m+{g_m}^2}{2\pi(Cg_{ds,1}+Cg_{ds,3}+Cg_m)} \quad (18)$$

The transistor dimensions resulting from the design are shown in Table I. It is important to note that the resulting widths and lengths were previously designed to produce an ultra-low-power voltage reference. The extracted flicker constants and transistor transconductances are also presented in Table I. The extraction of flicker constants was obtained from HSPICE simulations using curve fitting method along with Eq. (14).

TABLE II
THERMAL NOISE CONTRIBUTION OF EACH TRANSISTOR TO THE OUTPUT

Symbol	Transistor	Output noise	Percentage
$V_{w,M1}$	M1	67.98 μV	46.82 %
$V_{w,M2}$	M2	25.38 μV	6.53 %
$V_{w,M3}$	M3	67.86 μV	46.65 %
V_{wT}	M1+M2+M3	99.39 μV	100 %

The percentages refer to the square of each voltage noise, since their contributions to the output are added up quadratically.

In Fig. 5, it is possible to observe that the predicted results obtained from the proposed analysis are in close agreement with the simulations. As can also be observed in Fig. 5, the dominant pole frequency ($f_P = 11.11$ Hz) was assumed ideal, in the sense that noise frequency response above f_P is zero. The total noise produced by the simulation was 104.80 μV.

IV. CONCLUSIONS

In this paper analytical expressions were advanced to predict the thermal and flicker intrinsic noises of 3T voltage references. Simulation results showed that the developed modeling can predict the intrinsic noise with a relative error lower than 5%. The intrinsic noise of voltage references is an important performance parameter that limits the resolution of analog-to-digital and digital-to-analog converters. In fact, since the simulated total RMS noise (104.80 μV) represents 0.09% of the reference voltage (115 mV), a maximum resolution of 10 bits can be obtained.

ACKNOWLEDGMENT

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V. REFERENCES

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